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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,268	08/14/2006	Katsunori Asano	925-327	6483

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EXAMINER	
JAHAN, BILKIS	
ART UNIT	PAPER NUMBER
2814	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,268	ASANO ET AL.	
	Examiner	Art Unit	
	BILKIS JAHAN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-35* is/are pending in the application.

4a) Of the above claim(s) *18-24,26 and 29-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17, 25, 27, 28, 34-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/17/08, 03/19/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 17 is objected to because of the following informalities:

Claim 17 includes "a volume comprising the second base layer has **homogeneous impurity concentration**" but it is not clear the meaning of the homogeneous impurity concentration from claim language and specification.

Appropriate correction is required.

Inasmuch as understood in light of claim objection, the rejection as follows:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17, 25, 28, 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nobuyoshi et al (JP 08-204169) in view of Oikawa et al (5,021,855). The machine translation of JP 08-204169 has been used for the rejection and attached.

Regarding claim 17, gate turn-off thyristor of a wide-gap semiconductor (Fig. 1), comprising:

- a first emitter layer 5 (Fig. 1, Para. 13) comprising either one of n-type and p-type (Fig. 1, Para. 13) conductive types and having a first electrode 3 (Fig. 1, Para. 13) on its one surface (Fig. 1);
- a first base layer 7 (Fig. 1, Para. 13) comprising a conductive type different (Fig. 1) from that of the first emitter layer 8 and provided on the another surface of the first emitter layer 8;
- a second base layer 6 (Fig. 1, Para. 13) comprising a conductive type identical to that of the first emitter layer 8 and provided on the first base layer 7;
- a mesa-type second emitter layer 5 (Fig. 1, Para. 13) comprising a conductive type different from that of the first emitter layer 8 and provided on the second base layer 6 in a manner whereby a flat interface (Fig. 1) is formed between the second emitter layer 5 and the second base layer 6;
- a second electrode 2 (Fig. 1, Para. 13) provided on the mesa-type second emitter layer 5; a low-resistance gate region 10 (Fig. 1, Para. 37) embedded in the second base layer 6 below the interface and spaced away from the interface in a stacking direction (Fig. 1), the stacking direction being perpendicular to the interface (Fig. 1), the low- resistance gate region 10 comprising a conductive type identical to that of the second base layer 6 and an impurity concentration higher than that of the second base layer 6; and

- a third electrode 4 (Fig. 1, Para. 13) put in contact with the low-resistance gate region 10, wherein
- a volume comprising the second base layer 6 has homogeneous impurity concentration (Fig. 1, Para. 13), the volume extending between the interface (Fig. 1) and a lower layer upon which the second base layer 6 is formed.
- Nobuyoshi does not explicitly disclose a third electrode 4 put in contact with the low-resistance gate region 10 via a gate contact region.
- However, Oikawa discloses a third electrode 9 (Fig. 1B, col. 6, line 43) put in contact with the low-resistance gate region 6 (Fig. 1B, col. 5, lines 3, 20-27) via a gate contact region 6C (Fig. 4, col. 7, lines 57-58). Oikawa teaches the above modification is used to narrow the area of the cross section of one current path so that the influence of the control signal can be effectively given to all positions of the current path in the gate turn-off-thyristor (col. 1, lines 18-23). It would have been obvious to one of the ordinary skill of the art at the time of invention to add Nobuyoshi's structure with Oikawa's structure as suggested above to narrow the area of the cross section of one current path so that the influence of the control signal can be effectively given to all positions of the current path in the gate turn-off-thyristor (col. 1, lines 18-23).

Regarding claim 25, Nobuyoshi modified by Oikawa et al further disclose the first emitter layer is an n-type cathode emitter layer 5A-5B (Oikawa, Fig. 1B, col. 4, lines 57-59), the first base layer 4 (Oikawa, Fig. 1B, col. 4, line 42) is a p- type base layer, the second base layer is an n-type base layer 3 (Oikawa, Fig. 1B, col. 4, line 40), the second emitter layer is a p-type anode emitter layer 2 (Oikawa, Fig. 1B, col. 4, lines 38-39), and the low-resistance gate region is an n-type 6 (Oikawa, Fig. 1B, col. 5, lines 3, 20-27), and the first, second and third electrodes are a cathode electrode 8A-8C (Oikawa, Fig.1B), an anode electrode 7 (Oikawa, Fig. 1B) and a gate electrode 9 (Oikawa, Fig. 1B), respectively (Oikawa, Fig. 1B).

Regarding claim 28, Nobuyoshi modified by Oikawa et al further disclose an impurity concentration of the low-resistance gate region is three or more times an impurity concentration of the base region (Oikawa, col. 5, lines 33-35).

Regarding claim 34, Nobuyoshi modified by Oikawa et al further discloses the gate contact region 6C (Oikawa, Fig. 4) is located between the low-resistance gate region 6 (Oikawa, Fig. 1B) and the third electrode 9 (Oikawa, Fig. 4) with respect to the stacking direction perpendicular to the surface direction and is apart from the second emitter layer 5A-5C with respect to the surface direction, and has a conductive type identical to that of the second base layer (Oikawa, col. 5, lines 33-35). However, Nobuyoshi modified by Oikawa et al does not explicitly discloses the gate contact region 6C having an impurity concentration higher than an impurity concentration of the low-

resistance gate region. However, Oikawa discloses low-resistance gate region is three or more times an impurity concentration of the base region (Oikawa, col. 5, lines 33-35). It would have been obvious to one of the ordinary skill of the art at the time of invention to do the gate contact region 6C (Oikawa) having an impurity concentration higher than the low-resistance gate region 6 (Oikawa) to get better connection from gate electrode to the base layer of the thyristor.

- Also, it would have been obvious to one of ordinary skill in the art to **use any suitable impurity concentration for the device**, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Alner, 220 F .2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 35, Nobuyoshi further discloses an outer circumference pattern of the second emitter layer 5 is in correspondence with an inner circumference pattern of the low-resistance gate region 10 with respect to the surface direction.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nobuyoshi et al (JP 08-204169), Oikawa et al (5,021,855) and further in view of Edmond et al (5,539,217).

Regarding claim 27, Nobuyoshi in view of Oikawa et al discloses limitations above in claim 17 but do not disclose the wide-gap semiconductor is silicon carbide

(SIC). However, Edmond et al disclose the wide-gap semiconductor is silicon carbide (SIC) (Abstract). Edmond teaches SiC semiconductor is used to improve high thermal conductivity and high breakdown electric field in the device (col. 2, lines 25-28). It would have been obvious to one of the ordinary skill of the art at the time of invention to replace Nobuyoshi in view of Oikawa's structure with Edmond's structure including the wide-gap semiconductor is silicon carbide to improve high thermal conductivity and high breakdown electric field in the device (col. 2, lines 25-28).

Response to Arguments

Applicant's arguments with respect to claims 17, 25, 27, 28, 34-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BILKIS JAHAN whose telephone number is (571)270-5022. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wai-Sing Louie/
Primary Examiner, Art Unit 2814

BJ